1. A memory cell, comprising a gated diode having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said diode.

2. The memory cell of claim 1 wherein said gated diode is a four-region diode.

3. The memory cell of claim 2 wherein said four-region diode is a p-n-p-n diode, and the memory cell is linked to a second memory cell having a gated p-n-p-n diode so that the two p-n-p-n diodes share a common n-region.

4. The memory cell of claim 2 wherein said four-region diode is an n-p-n-p diode, and the memory cell is linked to a second memory cell having a gated n-p-n-p diode so that the two n-p-n-p diodes share a common p-region.

5. The memory cell of claim 2 wherein said four-region diode comprises two complementary planar bipolar transistors.

6. The memory cell of claim 1 wherein the gate of said gated diode overlies a central junction of said gated diode.

7. The memory cell of claim 1 wherein said gate-induced latch-up is achieved by a pulsed gate bias.

8. The memory cell of claim 1 wherein said cell is a static random access memory cell.

9. The memory cell of claim 1 wherein said cell has an area of approximately 8 to $10F^2$ where F is the minimum lithographic dimension.

10. The memory cell of claim 6 wherein p and n regions of said central junction have respective p and n dopant concentrations of at least about 10^{18} atoms per cm^3.

11. A circuit for storing information as one of at least two possible stable current states, comprising:

a multi-region thyristor having at least four regions; and

at least one gate in contact with a junction of said multi-region thyristor, wherein said gate is connected to a voltage source for producing latch-up in said multi-region thyristor.

12. The circuit of claim 11 wherein said latch-up provides one of the stable current states for storing information in said circuit.

13. The circuit of claim 11 wherein said latch-up is produced by providing positive voltage to said gate.

14. The circuit of claim 11 wherein said latch-up is produced by providing a pulsed bias to said gate.

15. The circuit of claim 11 wherein said multi-region thyristor comprises a seven-region thyristor.

16. The circuit of claim 15 wherein said at least one gate comprises a first gate overlying a second junction of the seven-region thyristor, and a second gate overlying a fifth junction of the seven-region thyristor.

17. The circuit of claim 16 wherein said circuit comprises two memory cells.

18. The circuit of claim 17 further comprising a shared row address line in connection with a central region of said seven-region thyristor.

19. The circuit of claim 11 further comprising a write row address line in connection with said at least one gate.

20. A SRAM array, comprising:

a pair of memory cells each having a four-region latch with a gate in contact with a central junction of said four-region latch, wherein said gate is connected to a voltage source for producing latch-up in said four-region latch; and

wherein said cells are linked so that the

four-region latches of each cell overlap to share a common region.

21. The SRAM array of claim 20 wherein said four-region latch is a p-n-p-n latch, and said cells share a common n region.

22. The SRAM array of claim 20 wherein said four-region latch is an n-p-n-p latch, and said cells share a common p region.

23. The SRAM array of claim 20 wherein said latch-up provides one of the bistable current states for storing information in said cells.

24. The SRAM array of claim 20 wherein said latch-up is produced by providing positive voltage to at least one of said gates.

25. The SRAM array of claim 20 wherein said latch-up is produced by providing a pulsed bias to at least one of said gates.

26. The SRAM array of claim 20 wherein said four-region latch comprises two complementary planar bipolar transistors.

27. The SRAM array of claim 20 further comprising a row address line in connection with the common region of said cells.

28. The SRAM array of claim 20 further comprising a write row address line in connection with the gate of each cell.

29. A SRAM array, comprising

a substrate;

a plurality of planar four-region transistors each having a gate overlying a central junction of said planar four-region transistors; and

gate lines connecting the gates to a voltage source for producing latch-up in said four-region transistors.

30. The SRAM array of claim 29 wherein said latch-up provides one of the stable current states for storing information in said planar four-region transistors.

31. The SRAM array of claim 29 further comprising an insulating material layer between each of said transistors and the substrate, horizontally isolating the transistors.

32. The SRAM array of claim 31 wherein said insulating material is an oxide.

33. A computer system, comprising

a processor; and

a memory circuit connected to the processor, the memory circuit containing at least one memory cell comprising a gated four-region diode having bistable current states for storing information, one of said current

states being achieved by operation of gate-induced latch-up of said four-region diode.

34. The computer system of claim 33 wherein the four-region diode is a p-n-p-n diode.

35. The computer system of claim 33 wherein the four-region diode is an n-p-n-p diode.

36. The computer system of claim 33 wherein two memory cells of said at least one memory cell are linked so that the two four-region diodes share a common region.

37. The computer system of claim 33 wherein said gated four-region diode comprises two complementary bipolar transistors.

38. The computer system of claim 33 wherein the gate of said gated four-region diode overlies a central junction of said gated four-region diode.

39. The computer system of claim 38 wherein said gate-induced latch-up is achieved by a pulsed gate bias.

40. The computer system of claim 33 wherein said memory cell is a static random access memory cell.

41. The computer system of claim 33 wherein said static random access memory cell has an area of

approximately 8 to $10F^2$ where F is the minimum lithographic dimension.

42. A method of storing a binary logic value comprising:

inducing latch-up in a gated diode.

43. The method of claim 42 wherein the step of inducing latch-up further comprises application of a pulsed gate bias.

44. The method of claim 43 wherein said pulsed gate bias is approximately one volt.

45. The method of claim 42 wherein the step of inducing latch-up further comprises inducement of carrier multiplication and breakdown in the gated diode.

46. The method of claim 42 wherein the step of inducing latch-up further comprises application of a positive voltage.

47. The method of claim 46 wherein said positive voltage is approximately one volt.

48. A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a junction of said multi-region planar thyristor; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor.

49. The method of claim 48 wherein said step of providing doped silicon regions further comprises forming a seven-region planar thyristor.

50. The method of claim 49 wherein said step of providing doped silicon regions further comprises forming a p-n-p-n-p-n-p planar thyristor.

51. The method of claim 50 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.

52. The method of claim 49 wherein said step of providing doped silicon regions further comprises forming two memory cells.

53. The method of claim 52 further comprising connecting a central region of said seven-region planar thyristor to a shared row address line.

54. The method of claim 48 wherein said step of providing doped silicon regions further comprises forming one memory cell.